ABSTRACT OF THE DISCLOSURE

A drive signal from an SSG drives a CCD through a delay circuit and the like. An imaging signal from the CCD is converted to a video signal in a CDS circuit, which is driven by a sample hold signal given through the delay circuit, and is converted to a video signal that can be displayed on a monitor through an A/D converter circuit, a video signal processing circuit and a digital encoder to be output. Here, by correcting phases of the imaging signal and the sample hold signal, length of a signal line is corrected. Also, since the delay circuit is constructed by being incorporated in a DSP for video signal processing, which includes a video signal processing circuit and the like, the construction is simplified. Thus, the number of parts is reduced, and it can be constructed inexpensively.